# 1401-1406 CORE STORAGE

Precautions :

a) Do not place books, boxes or other items on top of 1401. This disturbs air cooling. (See CEM SA22).

b) Always replace directly the storage gate card cover after changing the cards to maintain correct cooling air flow to SMS power cards.

c) Do not stop the clock in a cycle, the "Stop clock" is built to stop at Ø Ø Ø when no current flows through the cores.

d) Always adjust or check the 1401 and memory voltages if machine trouble appears.

e) Do not rotate address switches while maintaining the Enter key up. This can damage SMS decode switches. If the Enter switch does not return to OFF automatically, replace it as soon as possible.

f) Do not pull or replace SMS cards in storage gate when power is on.

g) Never stop the storage gate fan. When troubles in this area are suspected, check the fan for proper working.

h) Do not interchange SMS cards until the current sources and diverters have been checked with a scope (see paragraph "Core storage trouble analysis").

i) When working on core storage problems, avoid hanging clips or probes on the core unit itself. For example, if a sense line is to be scoped, place the probe at the input of the pre-sense amplifier rather than on the core unit itself.
Same for inhibit, addressing, etc. Scoping on the core unit itself should be done only when absolute necessary.

./.

CORE STORAGE TROUBLE INDEX

```
                          ┌──────────┐
                          │  CORE    │      NO    ┌──────────────┐
                          │ STORAGE  ├──────────► │  ?  THINK  ! │
                          │ TROUBLE  │            └──────────────┘
                          └────┬─────┘
                               │
                     ┌─────────────────┐
                     │     READ         │
                     │ " PRECAUTIONS "  │
                     │    PAGE 1        │
                     └─────────┬────────┘
                               │
      INTERMITTENT    ┌──────────────────┐    SOLID
   ┌──────────────────┤   INTERMIT       ├──────────────────┐
   │                  │  OR SOLID        │                  │
   │                  │  FAILURE         │                  │
   │                  └──────────────────┘                  │
```

CHECK **CORE STORAGE** **VOLTAGES** **PAGE 5 AND 6**	**CHECK** **CORE STORAGE** **VOLTAGES** **PAGE 5 AND 6**

```
             ONE BIT                                    ONE BIT
        ┌──────────────┐                          ┌──────────────┐
        │  ONE BIT     │──── ONE BIT    ONE BIT ──┤  ONE BIT     │
        │  OR          │                          │  OR          │
        │  ALL BITS    │                          │  ALL BITS    │
        └──────┬───────┘                          └──────┬───────┘
           ALL BITS                                  ALL BITS
        ┌──────────────┐                          ┌──────────────┐
  YES   │  SEVERALL    │                          │    ALL       │   YES
 ┌──────┤  POSITIONS   │                          │ POSITIONS OF ├──────┐
 │      └──────┬───────┘                          │  A BLOCK     │      │
 │          NO                                    └──────┬───────┘      │
 │                                                    NO                │
```

BAD CURRENT OR DIVERTER CARDS (PAGE 8 & FOLLOWING TIMING PULSES (PAGE 8 AND 19)	DECODE SWITCHES (PAGE 8 , 12 AND FOLLOWING)	BAD DECODE SWITCHES (PAGE 8, 12 AND FOLLOWING)	BAD CURRENT OR DIVERTER CARDS (PAGE 8 & FOLLOWING) TIMING PULSES (PAGE 8 AND 19)
INCORRECT DECODE OF MAIN STAR MATRIX FAILURES CURRENT PAGE 7 AND 18	INCORRECT DECODING OF MAIN STAR MATRIX FAILURES CURRENT PAGE 7 AND 18	SWITCH CORE M TRIX & ASSOCIATED CIRCUITS (PAGE 15) CORE STORAGE HIMSELF	MATRIX BIAS (PAGE 6) OR A LOT OF BAD DECODE SWITCHES (PAGE 12 & FOLLOWING

```
          4000    ┌──────────────┐                    ┌──────────────┐    4000
       ┌──────────┤   2000       │                    │   2000       ├──────────┐
       │          │  OR          │                    │  OR          │          │
       │          │  4000        │                    │  4000        │          │
       │          │ MEMORIES     │                    │ MEMORIES     │          │
       │          └──────┬───────┘                    └──────┬───────┘          │
       │              2000                                 2000                 │
```

SENSE AMPLIFIER AND 2nd AMPLIFIER (PAGE 8 , 16 AND 17)	INHIBIT DRIVE OR RESISTOR (PAGE 15)	INHIBIT DRIVES RESISTOR OR OPEN WIRE IN CORE STORAGE (PAGE 8 AND 15)	SENSE AMPLIFIER AND 2nd AMPLIFIER (PAGE 8 , 16 AND 17 CORE STORAGE HIMSELF

GENERAL FLOW OF CORE STORAGE
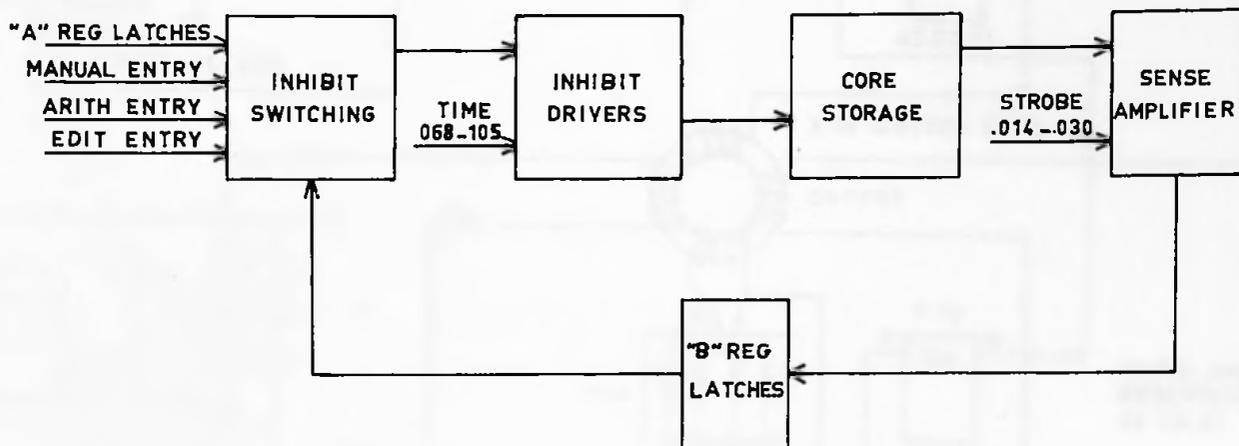
FIGURE A
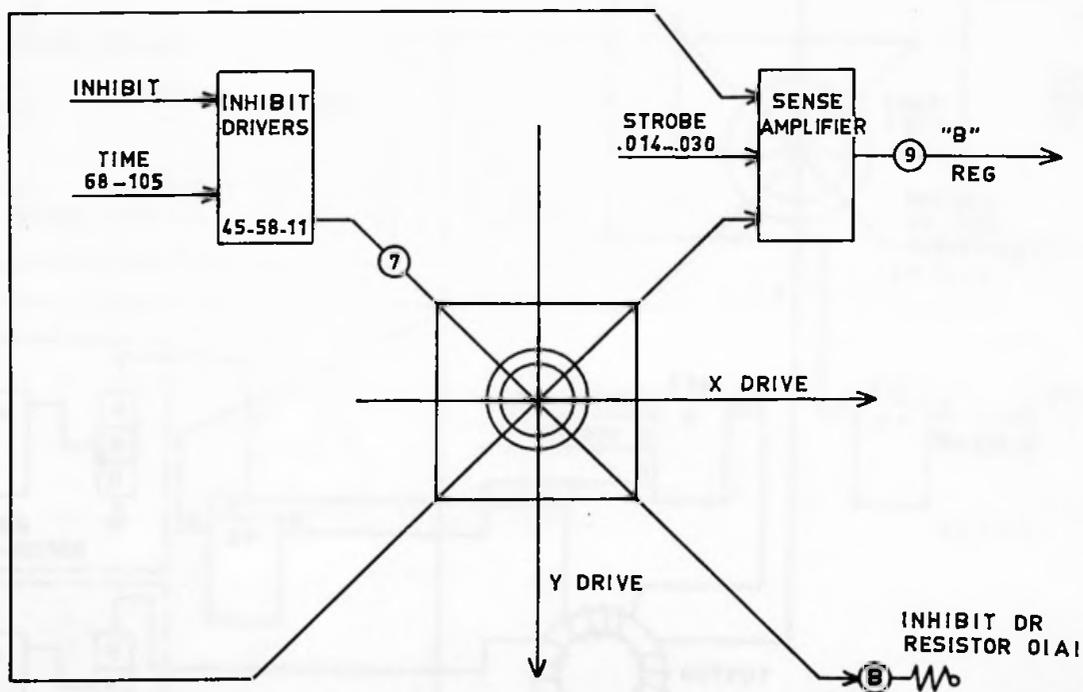
FIGURE B

COMPOSITE OF SWITCH CORE CIRCUITRY

FIGURE C

UNITS DECODE
42.53.11

EVEN HUNDS DECODE
42.55.11

F 14 DP
C   G
008-075 B
ACTIV. STOR G
42.57.11

F07
A   C

+ U INHIBIT DR
- U TIME 068-105
D   INHIBIT
42 58 11 INHIBIT DRIVER

STROBE014-030 H
PRE AMP   AMP   → TO B REG
A
C
42.59.11 SENSE AMPLIFIER

42 56 11 HUNDS AND THOUS-DECODE

42 54 11 TENS DECODE

ACTIV. STOR.B
F 08
D
A   C   R1
42.57.11

5 X 10 SWITCH CORE

OUTPUT

R 2

F 06
F   G

D 08
A

F 16
DP
C   G
42.57.11

CHOKE AND RESISTORS
42.40.41

CORE 1 BIT
X   Y

INHIBIT DR. RES.
42.40.43   + 12 V

CHOKE AND RESISTORS
42.40.41

ACTIV. STOR.G
F04
015-075 B
D   R3
A

F10 DP
C   G

F 12 DP
C   G

F 05
000-036 B
D   A
42.57.11

OUTPUT

8 X 10 SWITCH CORE

BIAS   + 30 V

<u>Checking and adjusting core storage voltages</u>.

<u>Be very careful</u> : when you adjust core storage voltages for shorting pins with uninsulated tips, this can damage SMS circuits which are difficult to debug.

<u>Stage 1 Systems</u>.

Adjust voltages as follows using <u>the best possible instrument</u> :

a) + 30V by checking at 01A1F26N.

b) Place deck 9100 in 1402 and run it, set switch **D** on and allow deck to run on all 4000 memories.

c) <u>Caution</u> : Do not exceed limits of + 10 and + 14 V when making the following :

Vary upwards + 12V memory voltage (check at pin 01A1F26Q) until machine fails, then vary downwards + 12V until storage or B register errors appear, note both voltages and place + 12V potentiometer value on center of range.
Write voltage recorded on decal near + 12V pot. normally the setting of + 12V should be within the limits of 11 to 13V. If the voltage is not within these limits bad current power drivers may be suspected.

d) For checking purpose vary the + 30V, + 1V and - 1V. The machine should run without any errors. Do not exceed 1,5 to 2 V range in both directions because this can decrease very quickly the life of the current drivers. Adjust Voltage again correctly after these checks.

Stage 2 and above.

Adjust voltages as follows using the best possible instrument :

a) + 30V by checking at 01A1F26N.

b) + 12V fix by checking at 01A1F26Q. (See power supply logic manual page 38.11.74 to find locations of these units).

c) Plug the marginal power supply into + 30 M and vary voltage + 1 and - 1 volt. Machine should run without any errors, you can vary up to 1,5 V to 2 V in both directions but do not exceed these limits because this will damage the driver cards. If errors occur on one side of + 30V mesure at 01A1F13Q and adjust + 18V differential (also knowed as + 12V variable) to have the same limits in both directions. Note that these limits must be at least + and -1 V. When the correct adjustments have been made note the voltage recorded on decal near 18V differential pot. If your system has a 1406, proceed exactly like on the 1401, but note that there is one + 30V supply for the 1406, one + 12V fix and one + 18V differential supply for 8 and 12K system, for a 16K there is a supplementary 18V differential supply for 06B5 storage gate. To vary the + 30V M on 1406 use portable marginal power supply, or if machine is equipped with a fixed marginal supply use the remote cable from 1401 REM (gate 02A4) to 1406. On 16K system two inputs for + 30V M are used in 1406 unit, normally the upper one is used for the gate 06B1 and the lower one for gate 06B5.

Note = + 30V BIAS after all matrix wires (measured at 01A2F06B on stage 2 and at 01A1F04C on stage 1. Will be + 26,5V approximately).

d) For checking purpose, after voltage adjustments it is possible to scope the current of the memory X and Y drivers by using a current probe and its adapter (PN 451213 and 451214) which are branch office tools. This probe will be set on scope, sync. on time Ø Ø Ø, set voltage input to 0,05 and the switch of the adapter to 2MA for 1MV. Probe on the wires of the terminal board behind the console (for example at corresponding point of units Ø and hundreds Ø for drive X. Set address switches of the console to Ø Ø Ø and shift enter key. Pattern should appear like on figure 1 or 2. The write current flow must be approximately 270 to 290 MA for stage 2 machines and 240 MA to 260 MA for stage 1 machines.

FIGURE 1
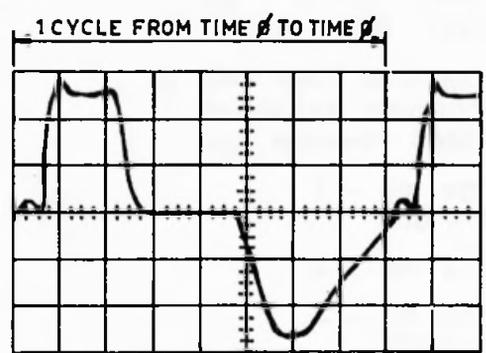
1 CYCLE FROM TIME Ø TO TIME Ø

VERT DEF   0,05 V PER DIV.

HORZ DEF   1 uS PER DIV UNCALIBRATED

SYNC   TIME Ø Ø Ø

TEST POINT   UNITS Ø-HUNDREDS Ø 1
MATRIX 5 X 10 FRONT PANEL

LOGIC

COMMENT   X DRIVE CURRENT. 275 MA

FIGURE 2
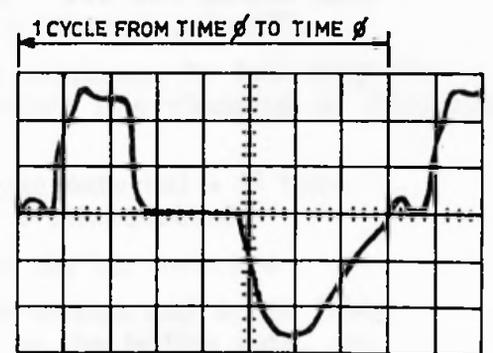
1 CYCLE FROM TIME Ø TO TIME Ø

VERT DEF   0,05 V PER DIV

HORZ DEF   1 uS PER DIV UNCALIBRATED

SYNC   TIME Ø Ø Ø

TEST POINT   TENS Ø-EVEN HUNDREDS
THOUSAND Ø MATRIX 8 X 10
FRONT PANEL

LOGIC

COMMENT   Y DRIVE CURRENT 275 MA

Core storage trouble analysis.

When troubles are suspected in the memory circuits, follow the instructions written on the paragraph "Precautions" and check the 1406 and memory voltage (if + 12V variable or 18V differential is not present see note 1). When the machine has a 1406 check if trouble appears on 000 to 3999, 4000 to 11999, or 12000 to 15999, check also if only one bit is failing, this means that the bug is located in the amplifier, inhibiting or core circuits itself.

Keep in mind that :

a) Picking up or dropping a specific bit in any location of a block of 4000 memories is normally caused by a poor sense amplifier, when suspected replace it.

b) Troubles appearing to a specific address can be pointed to be bad decode switches.

c) Troubles that cannot be pointed to a specific bit or location are normally caused by a poor current source or diverter card if only a block of 4000 memories is failing. If all are failing, check immediately time R1 - U 000 - 036. R2 - U 008 - 075. R3 - U 015 - 075. Strobe - T014 - 030 and inhibit time - U 068 - 105. (see paragraph "Core storage pulses").

d) SMS card damage can be held to a minimum by following the hereafter mentioned precautions before interchanging or swapping any memory SMS cards :

1 - Set up the scope and sync external + U time 000 - 030 speed sweep 1 microsecond.

2 - Set a valid character in the bit switches

3 - On alter mode hit enter switch and scope F04A, F05A, F07A and F08A on the failing gate, (on stage 1 machines these points are F10A, F12A, F20A and F22A).

Gate 01A1 for 0000 to 3999
Gate 06B1 for 4000 to 11999   in the 1406
Gate 06B5 for 12000 to 15999 in the 1406

4 - Compare the wave forms with the pictures 3 to 6. They represent the different points with time R1, R2, R3 or when the machine is not operating.

Note 1 - To avoid electrical and/or mechanical damage when an overload occurs, the + 30V input to the 18V differential power supply is now being fused. This 0,75 A fuse is located on the heat sink of the power supply itself and is not visible from the outside of the machine (gate 01A5 on model A or gate 02A5 on other models). Care should be taken for this trouble. This will be eliminated by installing B/M 485.823 which causes Power Off when this fuse blowns. This bill has been installed if the 18V differential power supply has a wire on terminal 5 (see CEM EC 895).

FIGURE 3
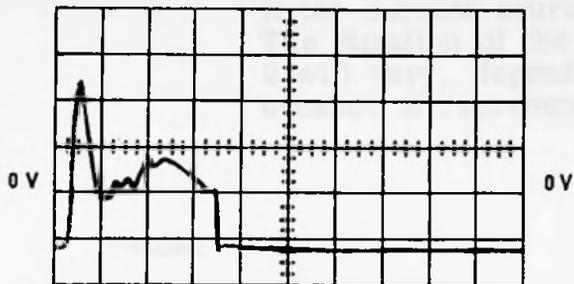
VERT DEF 10 V PER DIV

HORZ DEF 1 uS PER DIV

SYNC TIME ∅ ∅ ∅

TEST POINT F05A OR F08A (R1 TIME)

LOGIC 425711

COMMENT CORRECT CURRENT SOURCE

FIGURE 4
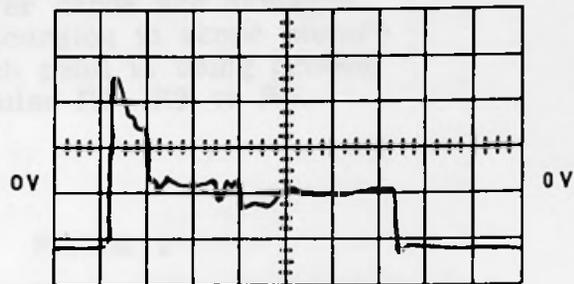
VERT DEF 10 V PER DIV

HORZ DEF 1 uS PER DIV

SYNC TIME ∅ ∅ ∅

TEST POINT F07A (R2 TIME)

LOGIC 425711

COMMENT Correct current source Enter key UP

FIGURE 5
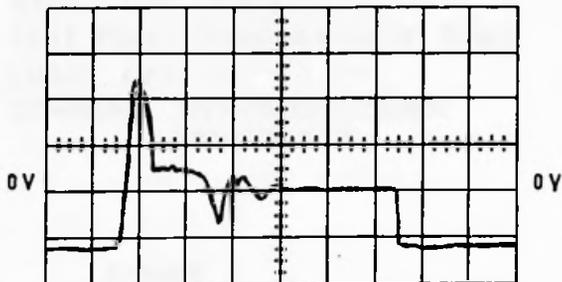
VERT DEF 10 V PER DIV

HORZ DEF 1 uS PER DIV

SYNC TIME ∅ ∅ ∅

TEST POINT F04A (R3 TIME)

LOGIC 425711

COMMENT CORRECT CURRENT SOURCE

FIGURE 6
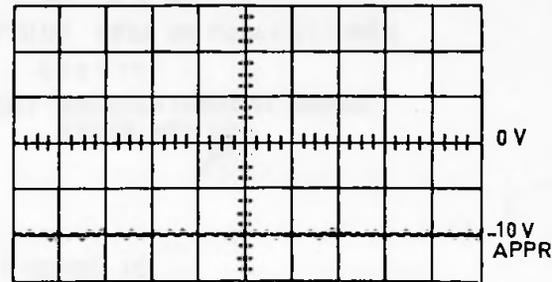
VERT DEF 5 V PER DIV

HORZ DEF 1 uS PER DIV

SYNC TIME ∅ ∅ ∅

TEST POINT F04A TO F08A

LOGIC 425711

COMMENT CORRECT CURRENT SOURCE ENTER KEY DOWN

Note - Test points are shown for stage 2 machines.
The equivalent for stage 1 machines are F04A = F10A,
F05A = F12A,
F07A = F20A,
F08A = F22A,

5 - If all pictures are correct the current source and diverter cards are working correctly unless highly intermittent failures, and in this case trouble will be on other circuits.

6 - Scope pictures 7 to 11 represent what will be seen
if the current source or diverter cards are damaged.
The duration of the positive excursion in scope picture
8 will vary, depending on which point is being probed,
because it represents timing pulse R1, R2 or R3.

FIGURE 7
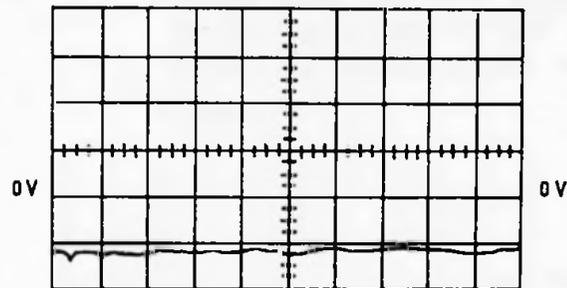
0 V   0 V

VERT DEF   10 V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT   FO5A OR FO8A (R1 TIME)
LOGIC   425711
COMMENT   OPEN CURRENT SOURCE
                ENTER KEY UP

FIGURE 8
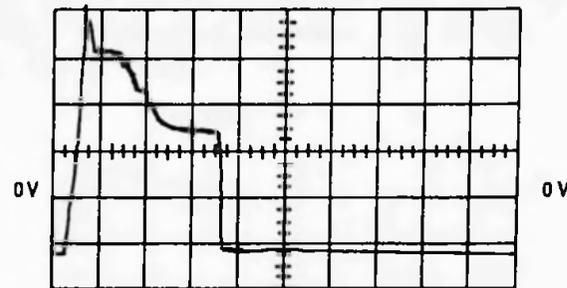
0 V   0 V

VERT DEF   10 V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT   F∅5A OR FO8A (R1 TIME)
LOGIC   425711
COMMENT   SHORTED CURRENT SOURCE
                ENTER KEY UP

FIGURE 9
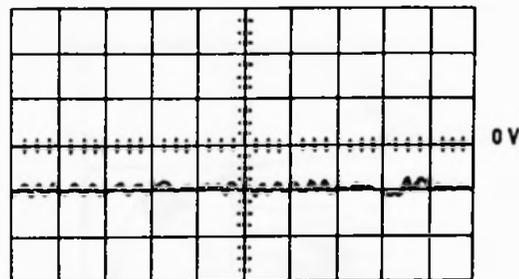
0 V

VERT DEF   5 V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT   FO4A TO FO8A
LOGIC   425711
COMMENT   SHORTED CURRENT SOURCE
   ENTER KEY DOWN

FIGURE 10
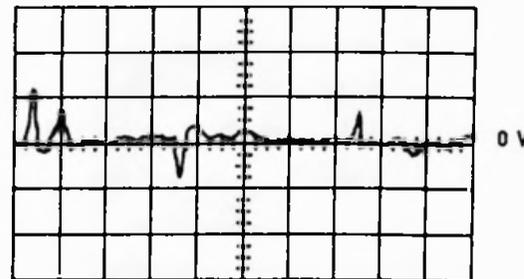
0 V

VERT DEF   10 V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT   FO4A TO FO8A
LOGIC   425711
COMMENT   OPEN DIVERTER CARD

If source or diverter trouble is indicated, proceed as follows :

By using the chart figure 27 or 28 locate corresponding current source card that correspond to the bad point scoped. Replace it. A good hint to find a bad current source is to feel with a finger the black resistor located on the end of SMS card from F10 to F16 (on stage 1 machines, F04, F07, F14, F17).
A very hot resistor (be very careful, do not burn your finger) will indicate a bad current source but, this is only true on stage 1 and stage 2 old style drivers (see figure 13A). If you want to replace old style drivers by new ones (stage 2 only) or if your replacement cards AQW are new models, you must add a capacity P/N 725.805 or its equivalent 75 MF 15 to 20V, connected between 01A1F13Q and 01A1F13J positive side on F13Q (CEM 1067).

FIGURE 11
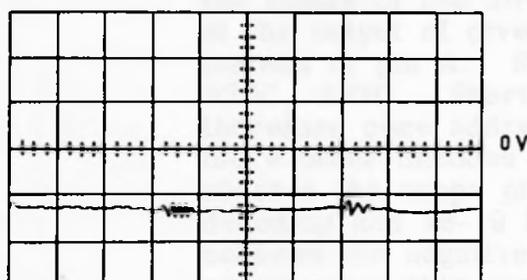
VERT DEF	10 V PER DIV
HORZ DEF	1 uS PER DIV
SYNC TIME	Ø Ø Ø
TEST POINT	F04A TO F08A
LOGIC	425711
COMMENT	SHORTED DIVERTER CARD

FIGURE 12
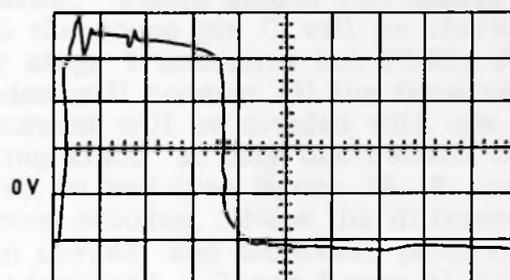
| VERT DEF | 10 V PER DIV |
HORZ DEF	1 uS PER DIV
SYNC TIME	Ø Ø Ø
TEST POINT	F05A OR F08A (R1 TIME)
LOGIC	425711
COMMENT	OPEN DECODE
	(SEE NOTE 2 ON NEXT PAGE)

HOT RESISTOR
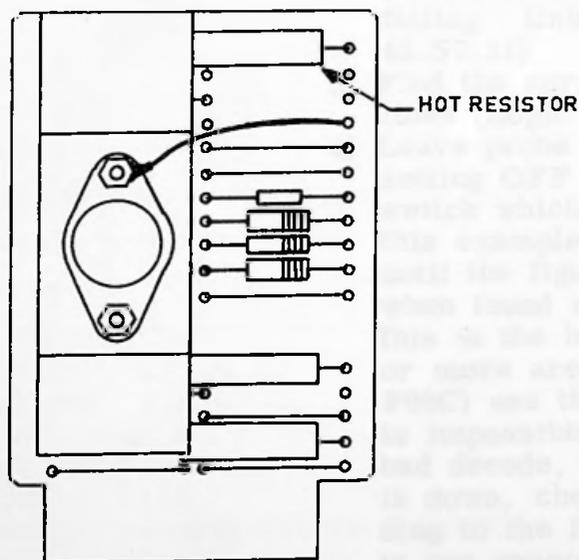
OLD STYLE

Figure 13A
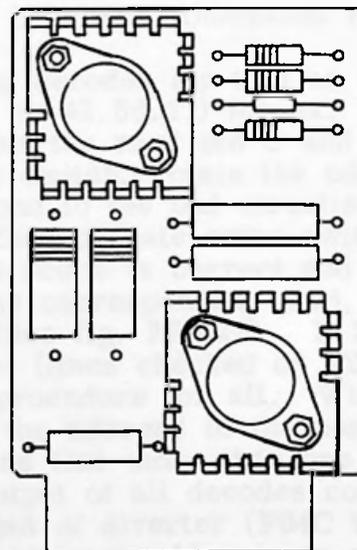
NEW STYLE

Figure 13B

7 - Always replace the current source card first, even if the
scope picture shows a bad diverter because most diverter
card damage is caused by the source cards. Recheck the
wave form after replacing the source card and if the pic-
ture is still wrong replace the diverter card.

8- Figure 12 represents an open decode card (See also figures
16 and 17). To locate it, use corresponding probe point
and contains of address switches (See note 2). In this
case replace bad decode switch.

9 - Shorted decodes do not appear on points F04A, F05A, F07A
and F08A. (See figures 14 to 19), because these points are
the inputs of the diverter cards. These shorts can appear
at the output of diverters so the scope pin C will be checked
instead of pin A. Same for stage 1 machines but F10C, F12C,
F20C, F22C. Shorted decodes will conduct all the time and
therefore core addressing current will be divided with one or
more other decodes conducting also. If only one decode is
shorted the scope picture will be bad (See figure 14-15, correct
decoding and 18-19 for shorted decodes. Note the difference
between the negative peak on correct and incorrect picture)
except when this decode is addressed. Check figure n° 27 or
28 to locate the bad SMS card.
Keep in mind that normally, only four decodes must be at
ground potential (conducting) and if you have difficulties to
locate which are the bad decodes, take the following procedure :

a) Set an address in main star where the core is
failing,
b) Hold up enter switch,
c) Check the outputs of diverter cards. (F04C, F05C,
F07C and F08C) to find which of the lines are
failing : Units, tens, hundreds, thousands (see
42.57.11)
d) Find the corresponding decodes for this or these
lines (Logic 42.53.11 to 42.56.11) for ex. : Units.
e) Leave probe tip on diverter card pin C and while
setting OFF the enter switch, rotate the address
switch which correspond to the bad circuits (in
this example units), then operate enter-switch again
until the figure of the scope is correct and
when found replace the corresponding card, because
this is the bad one. (See fig. 27, 28). If 2 lines
or more are incorrect (lines checked on F04C to
F08C) use the same procedure for all. When it
is impossible to find the address of the corresponding
bad decode, this means that more than one SMS card
is down, check the output of all decodes correspon-
ding to the faulty output of diverter (F04C to F08C) :
in our example it would be the 10 outputs of units
decode switch logic 42.53.11.

FIGURE 14
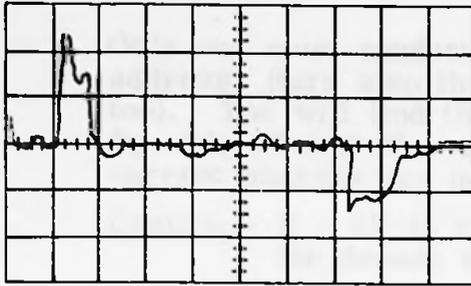
VERT DEF 10 V PER DIV
HORZ DEF 1 uS PER DIV
SYNC   TIME ∅∅∅
TEST POINT F04C OR F07C
LOGIC 425711
COMMENT CORRECT OUTPUT OF DIVERTER WHEN
ONE DECODE IS CONDUCTING (CENTER SWITCH ON)

FIGURE 15

0 V

VERT DEF 10 V PER DIV
HORZ DEF 1 uS PER DIV
SYNC   TIME ∅∅∅
TEST POINT F∅5C OR F∅8C
LOGIC 425711
COMMENT CORRECT OUTPUT OF DIVERTER WHEN
ONE DECODE IS CONDUCTING (ENTER SWITCH ON)

FIGURE 16
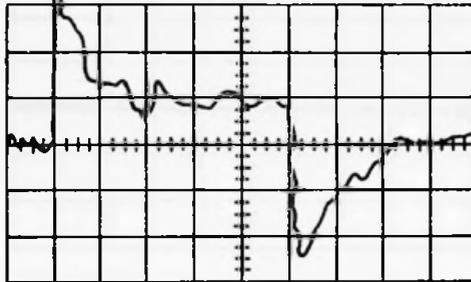
VERT DEF 10 V PER DIV
HORZ DEF 1 uS PER DIV
SYNC   TIME ∅∅∅
TEST POINT F04C OR F07C
LOGIC 425711
COMMENT NO DECODE SWITCH CONDUCTING

FIGURE 17
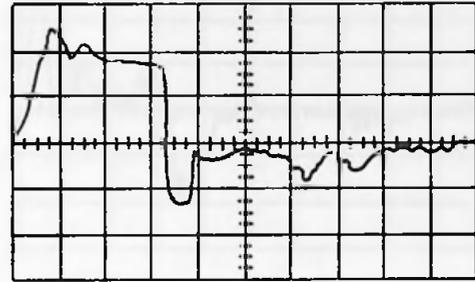
VERT DEF 10 V PER DIV
HORZ DEF 1 uS PER DIV
SYNC   TIME ∅∅∅
TEST POINT F05C OR F08C
LOGIC 425711
COMMENT NO DECODE SWITCH CONDUCTING

FIGURE 18
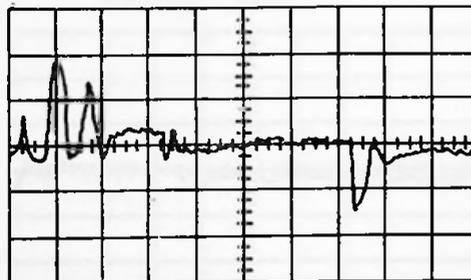
VERT DEF 10 V PER DIV
HORZ DEF 1 uS PER DIV
SYNC   TIME ∅∅∅
TEST POINT F04C OR F07C
LOGIC 425711
COMMENT 2 DECODES CONDUCTING (1 SHORTED)

FIGURE 19
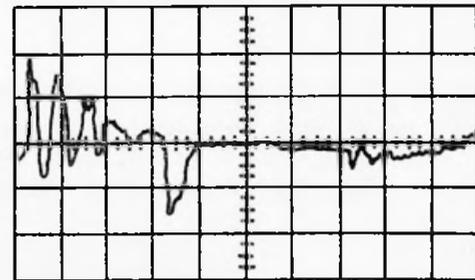
VERT DEF 10 V PER DIV
HORZ DEF 1 uS PER DIV
SYNC   TIME ∅∅∅
TEST POINT F05C OR F08C
LOGIC 425711
COMMENT 2 DECODES CONDUCTING (1 SHORTED)

Note specially that the negative
peak is shorter than on normal
decoding (figures 14 and 15).

Only one must conduct, the one that correspond to the console address, (turn also the switch to see if this output goes OFF too). You will find the correct and incorrect wave forms on fig. 20, 21 and 22. Replace all bad cards and check also if current sources are not damaged.

Caution - If - 6V is removed from storage gate you may burn out the decode switches.

Note 2 : Bad decode switches can damage the current source card clamping diode. Clamping diode or resistor damage in the source driver can be recognized by positive peak of + 42V instead of + 30V like shown on figures 3 to 5.

FIGURE 20
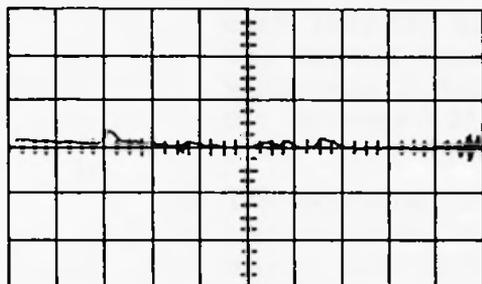
VERT DEF   10 V PER DIV
HORZ DEF
SYNC
TEST POINT UNITS ∅ (E 13 E)
LOGIC   4 2 5 3 1 1
COMMENT   DECODE SWITCH NORMALLY
                      CONDUCTING

FIGURE 21
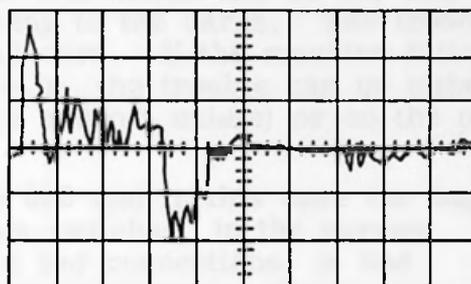
VERT DEF   10V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT UNITS 1 (E 13 P)
LOGIC   4 2 5 3 1 1
COMMENT   DECODE SWITCH NORMALLY
                      NOT CONDUCTING

FIGURE 22
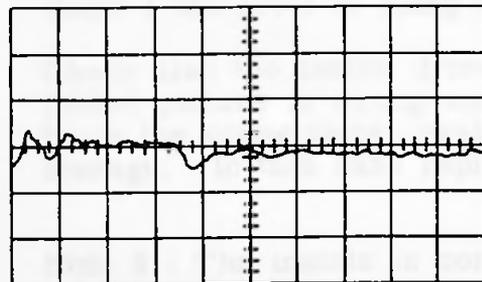
VERT DEF   10 V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT   UNITS ∅ (E 13 E)
LOGIC   4 2 5 3 1 1
COMMENT   SHORTED DECODE ALWAYS
                      CONDUCTING (NOT ADDRESSED)

10 - Do not forget that there exists a matrix of switch cores and a resistor on each driver lines and that the fault, in case of open lines, can be in this area (See note 3, Figure C and paragraph : other causes of intermittent failures).

11 - On stage 1 machines, to check if storage has bad decode switches, press power OFF and remove all decode cards (logic 42.53.11 to 42.56.11) except those used for address 000 (gate 01A1E03, E08, E12, E17). Set power on and try to enter in location 000.

Two results are possible :

a) The machine is working and in this case the bad decode will be normally in the removed cards (except if one of the four cards is shorted).
Return to their place the next four cards and so on, and try each possible address pertaining to the cards. The trouble will appear again with the bad card. If the machine fails when only 8 decode cards are in, the trouble can be either on the decodes addressing 000 (if a short exists) or on the other ones. Try by elimination.

b) The machine fails at address 000 and in this case the bug can be either in the 4 decodes switches, in the current source and diverter cards, in bad connections, in bad matrix or in matrix terminating resistors. Check with scope picture 3 to 6 to see if current source and diverter are working correctly, and if so, replace the 4 decodes with new cards and eliminate the bad ones.

Sense Amplifier and Inhibit checking.

If only one bit is missing or extra, check if machine works above or under 2.000 on the corresponding block, this can show a bad inhibit driver. The normal picture of inhibit driver can be seen on figures 23 and 24. Note that pictures are taken from stage 2 machines; on stage 1 the level is going from - 6V to + 6V.

Check also the inhibit drive resistor and correct soldering wires. If inhibit picture is wrong and the card has been replaced the fault will be in the connections, resistor or inhibit line itself inside the core storage. In this case replace the complete unit. (See page 22).

Note 3 : The matrix is composed by 2 plates with 10 x 10 switch cores and if a winding is open, you can switch the complete serie where the open switch is found to another one. Solder all wires to an unused one (see logic 42.40.21 and 42.40.31). This saves customer time and you can replace it on next P.M.

FIGURE 23
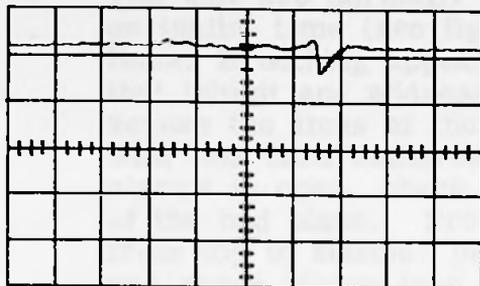
VERT DEF   5 V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT F 19 G (BIT 2) STAGE 2
LOGIC   42 58 11
COMMENT OUTPUT OF INHIBIT DRIVER
 (NOT CONDUCTING) BIT ENTERED

FIGURE 24
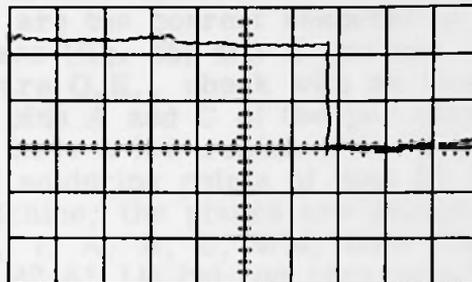
VERT DEF   5 V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT F 19 F (BIT 1) STAGE 2
LOGIC   42 58 11
COMMENT OUTPUT OF INHIBIT DRIVER
  THIS BIT IS NOT ENTERED (CONDUCTING)

FIGURE 25
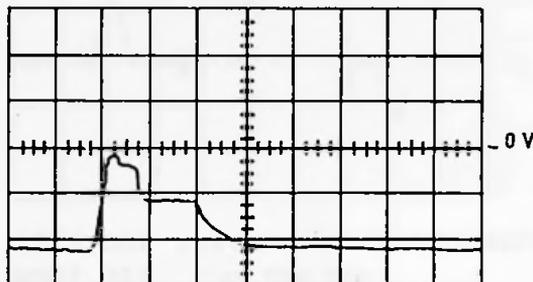
VERT DEF   5 V PER DIV
HORZ DEF   1 uS PER DIV
SYNC   TIME ∅ ∅ ∅
TEST POINT D 07 F (BIT 2)
LOGIC   42 59 11
COMMENT OUTPUT OF PRE-SENSE AMP.

If inhibit is O.K. and only one bit fails, the fault can be on sense amplifier or on core storage itself. Switch sense amplifiers with other ones (Logic 42.59.11) and if still wrong, scope the sense output by pulling the inhibit driver card for that bit (42.58.11). Each time the core is addressed, there should be an output on the pre-sense amplifier (see fig.25). If not, you can check the core output itself by using a double input scope with direct probes in differential amplifier, putting the probes on each side of the sense wires (on gate 01A1 inputs to the pre-sense amplifier) with the ground of probes and scope on pin J of this card, and setting the scope on vertical amplifier to 0,05 volts per division, and the mode "Added" with one channel inverted.

The ground of the scope power cord must be isolated to prevent noises.

You will see normally one pulse on strobe time and one inverted pulse on inhibit time (see fig. 26). They are the correct response of sense lines. If nothing appears except noises (fig. 25) and if you are sure that inhibit and addressing circuits are O.K., check with an ohmmeter across the lines at the lines at the pins A and C of the pre-amplifier with this card removed. You must have a low resistance. If your circuit is open, check wrapping and soldering points of pins 52 and 54 of the bad plane. Front side of machine, the planes are designed from top to bottom, planes 8, 4, 2, 1, A, B, C, WM, then row bits and check planes (see 42.59.11 and 42.41.11) but be very careful for counting wires and planes. If soldering points are correct and the circuit still open the core unit is bad and must be replaced (see page 22).

FIGURE 26
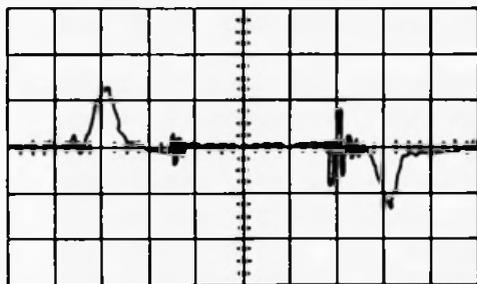
VERT DEF 0,05 V BOTH CHANNELS DIRECT PROBES

HORZ DEF 1 us PER DIV

SYNC TIME ∅ ∅ ∅

TEST POINT 0 1 A 1 D 0 4 A AND C

LOGIC 42.59.1.1.

COMMENT FERRITE CORE SENSE LINE RESPONSE
(MODE ADDED WITH ONE CHANNEL INVERTED)

Other causes of intermittent storage failures.

Intermittent storage failures can also be caused by faulty converters or inverters between the storage address latches and the memory address decodes. Check the address register signals to the storage decode switches in storage scan mode by sync on address stop and scope the edge connectors on the failing gate (01A1, 06B1 or 06B5). All signals should be at + U level 1 microsecond before time 000. Symptoms of this failure appear normally on customer programs by dropping some bits at storage read out, but memory works correctly when you try this position in enter mode or storage display. Matrix itself can also be incriminated but keep in mind that when determining a failure of matrix, what appears to be working is actually failing.

That is, if 50 addresses are failing, the 8 x 10 matrix output is bad and if 80 addresses are defective the 5 x 10 matrix is bad.

Do not forget that current required to flip cores varies according to room temperature, therefore if bits are missing, increase slightly the difference between + 30V and + 12V (18V differential for stage 2 machines) and if the machine has extra bits troubles, decrease the difference between both voltages, but in any case set + 30V to + 30 and then vary + 12V supply because in stage 2 machines + 12V (18 V differential) is referenced to + 30V.

Core storage pulses.

The timings of storage check pulses are listed as follows :

R1 time	- U 000 - 036	01A1F02A (Edge connector)
R2 time	- U 008 - 075	01A1F02B
R3 time	- U 015 - 075	01A1F02C
Strobe time	- T 014 - 030	01A1F02D
Z1 inhibit time	- U 068 - 105	01A1
Z2 inhibit time	- U 068 - 105	01A1

The delay cards to adjust these timings are located in gate 01B3 logic 31.12.93.2 (Logic 31.11.61.1). The delay card used is adjustable in 0,2 microsecondes steps from 0,2 to 1 microseconde. The location of these cards and their functions are :

Stage 2 machines

C06 delays the rise of - U R1
C07 delays the fall of - U R2
C09 delays the rise of + T, time 068 - 105
C08 delays the fall of - T, stobe time
014 - 030

To adjust the delay, change the output wire of the delay block to a pin location that will give the desired delay. Record the change on the system logics. Be very careful when adjusting the delay because some lines are delayed twice and varying the first will modify the other line too. When adjusting the delays observe the following tolerances : logic 42.40.53.2

Storage Pulse	Time in microsec. after TR1
- U 000 - 036 R1	3,7 $\pm$ 0,2 trailing edge
- U 068 - 105 Z1	6,8 $\pm$ 0,1 leading edge
- U 068 - 105 Z2	6,8 $\pm$ 0,1 leading edge
- U 008 - 075 R2	0,8 $\pm$ 0,2 leading edge
- T 014 - 030 strobe	1,7 $\pm$ 0,2 leading edge

These timings are referenced to the fall of - TR1 on 01B3A16F stage 2 machines (Logic 31.10.11) and the delays are measured at 50% level.

Normally the adjustments of the timing pulses are only done in the Factory.

20. -

| 0000 - 3999 GATE 01A1 | | | | | | | | 4000 - 7999 GATE 06B1 | | | | | | | |

ADDRESS	DECODE	DIVERTER	CURRENT SOURCE	ADDRESS	DECODE	DIVERTER	CURRENT SOURCE	ADDRESS	DECODE	DIVERTER	CURRENT SOURCE	ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
XXX0	E13			01XX				XXX0	E13			41XX			
XXX1	E13			03XX				XXX1	E13			43XX			
XXX2	E14			05XX	E09			XXX2	E14			45XX	E09		
XXX3	E14			07XX				XXX3	E14			47XX			
XXX4	E15	F08	F16	09XX				XXX4	E15	F08	F16	49XX			
XXX5	E15			10XX				XXX5	E15			50XX			
XXX6	E16			12XX				XXX6	E16			52XX			
XXX7	E16			14XX	E10			XXX7	E16			54XX	E10		
XXX8	E17			16XX				XXX8	E17			56XX			
XXX9	E17	(F22)	(F17)	18XX				XXX9	E17			58XX			
XX0X	E04			11XX				XX0X	E04			51XX			
XX1X	E04			13XX				XX1X	E04			53XX			
XX2X	E05			15XX	E10			XX2X	E05			55XX	E10		
XX3X	E05			17XX				XX3X	E05			57XX			
XX4X	E06	F05	F12	19XX				XX4X	E06	F05	F12	59XX			
XX5X	E06			20XX				XX5X	E06			60XX			
XX6X	E07			22XX				XX6X	E07			62XX			
XX7X	E07			24XX	E11	F04	F10	XX7X	E07			64XX	E11	F04	F10
XX8X	E08			26XX				XX8X	E08			66XX			
XX9X	E08	(F12)	(F07)	28XX				XX9X	E08			68XX			
X0XX	E18			21XX				X0XX	E18			61XX			
X1XX	E18			23XX				X1XX	E18			63XX			
X2XX	E19			25XX	E11			X2XX	E19			65XX	E11		
X3XX				27XX				X3XX				67XX			
X4XX	E19	F07	F14	29XX				X4XX	E19	F07	F14	69XX			
X5XX				30XX				X5XX				70XX			
X6XX	E20			32XX				X6XX	E20			72XX			
X7XX				34XX	E12			X7XX				74XX	E12		
X8XX	E20			36XX				X8XX	E20			76XX			
X9XX		(F20)	(F14)	38XX				X9XX				78XX			
00XX	E09	F04	F10	31XX				40XX	E09	F04	F10	71XX			
02XX				33XX				42XX				73XX			
04XX				35XX	E12			44XX				75XX	E12		
06XX				37XX				46XX				77XX			
08XX		(F10)	(F04)	39XX		(F10)	(F04)	48XX				79XX			

SMS CARD LOCATIONS FOR 10000 SERIES. DIVERTER & SOURCE CARDS IN PARENTHESIS—SUBTRACT ONE FOR DECODES. EX: E13 IS E12 ON 10000 SERIES

Figure 27.

8000 - 11999 GATE 06B1 **12000 - 15999 GATE 06B5**

8000 - 11999 GATE 06B1

ADDRESS	DECODE	DIVERTER	CURRENT SOURCE	ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
XXX0	E13			81XX			
XXX1	E13			83XX			
XXX2	E14			85XX	E09		
XXX3	E14			87XX			
XXX4	E15	F08	F16	89XX			
XXX5	E15			90XX			
XXX6	E16			92XX			
XXX7	E16			94XX	E10		
XXX8	E17			96XX			
XXX9	E17			98XX			
XX0X	E04			91XX			
XX1X	E04			93XX			
XX2X	E05			95XX	E10		
XX3X	E05			97XX			
XX4X	E06	F05	F12	99XX			
XX5X	E06			100XX			
XX6X	E07			102XX			
XX7X	E07			104XX	E11	F04	F10
XX8X	E08			106XX			
XX9X	E08			108XX			
X0XX	E23			101XX			
X1XX	E23			103XX			
X2XX	E24			105XX	E11		
X3XX	E24			107XX			
X4XX				109XX			
X5XX	E24	F07	F14	110XX			
X6XX	E25			112XX			
X7XX	E25			114XX	E12		
X8XX	E25			116XX			
X9XX	E25			118XX			
80XX				111XX			
82XX				113XX			
84XX	E09	F04	F10	115XX	E12		
86XX				117XX			
88XX				119XX			

12000 - 15999 GATE 06B5

ADDRESS	DECODE	DIVERTER	CURRENT SOURCE	ADDRESS	DECODE	DIVERTER	CURRENT SOURCE
XXX0	E13			121XX			
XXX1	E13			123XX			
XXX2	E14			125XX	E09		
XXX3	E14			127XX			
XXX4	E15	F08	F16	129XX			
XXX5	E15			130XX			
XXX6	E16			132XX			
XXX7	E16			134XX	E10		
XXX8	E17			136XX			
XXX9	E17			138XX			
XX0X	E04			131XX			
XX1X	E04			133XX			
XX2X	E05			135XX	E10		
XX3X	E05			137XX			
XX4X	E06	F05	F12	139XX			
XX5X	E06			140XX			
XX6X	E07			142XX			
XX7X	E07			144XX	E11	F04	F10
XX8X	E08			146XX			
XX9X	E08			148XX			
X0XX	E18			141XX			
X1XX	E18			143XX			
X2XX	E19			145XX	E11		
X3XX	E19			147XX			
X4XX				149XX			
X5XX	E19	F07	F14	150XX			
X6XX	E20			152XX			
X7XX	E20			154XX	E12		
X8XX	E20			156XX			
X9XX	E20			158XX			
120XX				151XX			
122XX				153XX			
124XX	E09	F04	F10	155XX	E12		
126XX				157XX			
128XX				159XX			

Fig. 28

Procedure to replace core storage assembly.

a - Remove all power from machine.

b - Remove the edge connectors Row G under core storage : these edge connectors are coming from 1402 (Brushes Row bits) and 1403 (Hammer response) if no print buffer is installed.

c - Remove edge connectors from rows D, E and F.

d - Remove the voltage wires from the two terminal blocks on rear of machine behind switch core matrix. In case of old style core storage the voltage wires are to be removed on the bottom of the core-unit mounting bracket. The unit must be tilted to the rear for better access to this block and therefore the wires are to be removed later on, when the points a to i are done.

Caution : Label the location of each wire removed to insure correct reconnecting. This is important because reversing the voltage leads can cause damage to the core array.

e - Remove the wires from the fan and the thermal switch.

f - Remove the metering unit and the convenience outlet box. (If you have more than one system the machine is equipped with an emergency power off, remove then the plug support behind the core storage).

g - Remove the four screws from the top of the core frame. These screws are holding the muffin fan support and the block itself.

h - Remove the fan unit.

i - Facing the front of the machine (console side), remove the two screws on the lower right - hand side of the core-unit mounting bracket.
Caution : Hold core-unit assembly when removing those screws.

j - Raise core-unit to disengage the left lower hand pin and remove the unit from the side of the cube.

k - Replace core-unit by following the reverse order.

l - Check the marginal limits of storage to find new limits.
Note these limits on decal near power supply (see paragraph : adjustments of core storage voltages).

-o-O-o-

FINAL TESTS

Vibration test for models A, B, C, E, F.

The card-decks for the vibration test have been established so, as to have a special deck numbered alike for each gate to be tested.

The different programs include instructions, which, as far as possible, test all circuits in the gate to be shaken, even if they do not allways result in logic functions. A correct use of these test-decks helps to cut down to a minimum the time spent for the vibration test and to locate a maximum of failures.

These test-decks are not appropriate to trace errors. They are only giving indications as to the good or bad quality of the SMS cards.

During the vibration test the "Input-Output Check Stop Switch" and the "Check Stop Switch" must be "ON". The test programs run until a "Stop Key" is depressed. The programs may be addressed by "420" unless the instructions given for a deck are different.

If no other indications are given, the noise of the Printer should reveal the good working of the machine.

Processing

1401 Basic + optional feature

GATE 01A3
===========

The following Sense Switches must be set to "ON".
Sense Switch C - for column binary
Sense Switch D - for 1406 coupling
Sense Switch E - for multi-div.
Sense Switch F - for advanced program
Sense Switch G - for expanded edit

Test : Load deck 01A3. Put cards with all possible bit combinations in the Reader. Blank cards in the Punch, depress Start Key and shake the gate.

./.

GATE 01A4   - 01A5
===========   ====

No Sense Switches are necessary.

Test :   Load Deck N° 0104 and shake gates 01A4 and 01A5

GATE 01A6
===========

No Sense Switches to "ON"

Test :   Load Deck 01A6. Blank cards in Reader and Punch. Depress
Start Key and Shake.

GATE 01A7
===========

Following Sense Switches "ON"

Sense Switch B - for type 4K
Sense Switch C - for machine 8K
Sense Switch D - for machine 12K and 16K
Sense Switch F - for advanced program

Test :   Load Deck 01A7. Blank cards in Reader and Punch.
Start Key and shake gate 01A7.

GATE 01A8
===========

The following Sense Switches to "ON"

Sense Switch B - for machine 4K
Sense Switch B, C - for machine 8K
Sense Switch B, C, D - for machine 12K
Sense Switch B, C, D, E - for machine 16K

Test :   Load Deck 01A8. Blank cards in Reader and Punch.
Start Key and shake.

GATE 01B1
============

The following Sense Switches to "ON"

Sense Switch B - for model C; load tape 1 and switch to ready
Sense Switch D - for 1406 coupling (8, 12 or 16 K)
Sense Switch E - for Mult-div.
Sense Switch F - advanced programming
Sense Switch G - Read-Punch release

Carriage Tape all Holes

Test :   On type 1403 carriage switch to "Neutral"
Load Test 01B1. Blank cards in Reader and Punch.
Start Key and shake.
After the Test put switch back to "IN".
Blank cards must be ejected to pockets "N" and "1".
If carriage tape stops, some failure is revealed.

GATE 01B2
============

The following Sense Switches to "ON"

Sense Switch C - for column binary
Sense Switch D - for 1406

Test :   Load deck 01B2. Blank card in Reader and Punch.
Start Key and shake.
Cards are ejected to pocket 4.
Attention : the last card is ejected into stacker "1".

GATE 01B3
============

The following Sense Switches to "ON"

Sense Switch E - for Multi-Div.
Sense Switch F - for advanced programming

Test :   Load deck 01B3. Blank cards in Reader and Punch.
Start and shake.

./.

GATE 01B4
============

The following Sense Switches to "ON"

Sense Switch B - for Punch Feed Read
Sense Switch C - for Column Binary
Sense Switch G - for Read Punch Release

Test :   Load deck 01B4. Cards with A8 in all columns into Reader
and Blank Cards into Punch. Start and shake. Program
with address "600".
Cards are punched A8 and ejected into all pockets. The
Printer runs also. Cards into Punch N only if column
binary or PFR (Switch "B", switch "C") are running also.

GATE 01B5
============

No Sense Switches to "ON"

Test :   Load card 01B5 and shake.
The Program can be reloaded with 062.

Attention : the hammer-drive cards must not be touched.

GATE 01B6
============

The following Sense Switches to "ON"

Sense Switch B - for High-Low-Equal
Sense Switch C - for Column Binary
Sense Switch G - for Exp. Edit

Test :   Load deck 01B6 and shake.

GATE 01B7 - 02A8
============   =====

The following switches to "ON"

./.

Sense Switch B - for High-Low-Equal
Sense Switch C - for Punch Feed Read
Sense Switch D - for Ramac
Sense Switch G - for Inquiry

Test :   Load deck 01B7. Cards with A8 in all columns for recent
machines, 60 or 40 for earlier machines into Reader and
blank cards into Punch. Start and shake.
All cards must be examined for identical punchings. For
PFR put also cards with A8 punchings. A punch 4 will be
added.

GATE 02A7 - 02B7
===========   =====

The following Sense Switches to "ON"

Sense Switch B - for 8K type
Sense Switch G - for 12K and 16K types

Test :   Load deck 02A7. Start and shake.

GATE 02B6   (not for machine 1, 4K)
===========

The following Sense Switches to "ON"

Sense Switch B - for 8K types
Sense Switch B, C - for 12 K types
Sense Switch B, C, D - for 16K types
Sense Switch F - for Indexing (avanced programming)
Sense Switch G - for compressed tape

Test :   Reset Storage
Load deck 02B6. Tape unit 1 load and ready. Start key
and shake. If the machine stops, there are failures.

GATE 02B8   (only for column binary added)
===========
No Sense Switches to "ON".

./.

Test :   Load deck 02B8. Detail cards with all signs (from Punch Column Binary) in Reader and blank cards in Punch. Start and shake.

Cards are punched in form of column binary. The Printer does not run. Program can be set by '600'.

-o-o-o-